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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,913	07/31/2001	Hitoshi Ikeda	100353-00065	2024

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EXAMINER
YOHA, CONNIE C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,913	IKEDA ET AL.	
	Examiner	Art Unit	
	Connie c. Yoha	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-10,13 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-10,13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. The Response filed on 11/18/02 has been entered and are made of record.

2. Claims 8-10 and 13-14 are pending.

3. References Maesako et al, Pat. No. 6016280 and Sakata et al, Pat. No. 5606265 (cited in previous office action) are used for a second non-final rejection of the pending claims.

Claim Rejections - 35 USC 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8-10 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maesako et al, Pat. No. 6016280 in view of Sakata et al., Pat. No. 5606265.

With regard to claim 8, Maesako discloses an SRAM memory block provide on a chip, the SRAM memory block including an SRAM cell array (fig. 83, 602); and a DRAM memory block provided on the chip, the DRAM memory block including a DRAM cell

array (fig. 83, 601). Maesako does not discloses a source voltage is externally supplied to the DRAM memory block when the DRAM cell array is accessed, and said source voltage to the DRAM memory block is set to a ground voltage when the DRAM cell array is not accessed. However, Sakata discloses a method in which a source voltage (Vch) is applied to the power line to a word driver of the DRAM memory block when the DRAM cell array is accessed, and setting the source voltage to ground (vss) when the word line of the DRAM cell array is in a nonselected state (col. 10, line 57-62) (fig. 1, 3, 5A) for the purpose of reduce waste current when the memory cell array is not in use. Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to combine the Maesako's device with Sakata's having a source voltage (Vch) supplied to the memory block when it is being accessed and setting the source voltage to ground when it is inaccess so as to reduces the waste current, thus the operation speed is lowered and power consumption is improved (also with regard to claim 14).

With regard to claim 9, Maesako discloses an inherent first power pad for receiving an SRAM source voltage (fig. 83, VINT2), the SRAM source voltage being supplied from the first power pad to the SRAM memory block (fig. 83, 602); an inherent second power pad for receiving a DRAM source voltage (fig. 83, VINT1), the DRAM source voltage being supplied from the second power pad to the DRAM memory block (fig. 83, 601).

With regard to claim 10, Maesako discloses an inherent power pad (pad at receiving fig. 83, Vext) shared by the SRAM memory block (fig. 83, 602) and the DRAM

memory block (fig. 83, 601), the power pad receiving the externally supplied source voltage (fig. 83, VEXT (EXTERNAL POWER SOURCE VOLTAGE TERMINAL); and a control unit for controlling ON/OFF of the source voltage supplied from the power pad to the DRAM memory block in response to a control signal which is externally supplied to the control unit (fig. 83, 603) (also with regard to claim 13)

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicants disclosure Takata et al (5828596) and Matsuo et al (5781468) disclose a memory device.

6. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 306-5731. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 308-7722. Any inquiry of a general nature or

relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

C. Yoha

January 2003